

#### Hex Inverter Gate with LSTTL compatible inputs in bare die form

Rev 2.0 10/08/25

#### Description

The 74ACT04 hex inverter gate is fabricated using an advanced 5V CMOS process to combine high speed LSTTL performance with CMOS low power. The device contains six independent inverters which perform the Boolean function  $Y = \bar{A}$ . Internal circuitry comprises of three stages and includes buffered output for high noise immunity and stability. Inputs are directly compatible with both standard TTL and CMOS outputs. All inputs are protected against ESD and excess voltage transients

# Ordering Information

The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54ACT04 REV 2

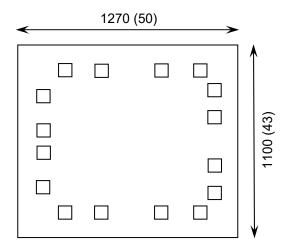
#### **Supply Formats:**

- Default Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 280µm(11 Mils) On request
- Assembled into Ceramic Package On request

#### Features:

- Inputs directly accept TTL
- Outputs directly interface CMOS, NMOS and TTL
- Outputs Source/Sink 24 mA
- Low Input Current: 1µA
- Functionally compatible with bipolar 74LS04
- Lower power alternative to bipolar logic.

#### Die Dimensions in µm (mils)



#### **Mechanical Specification**

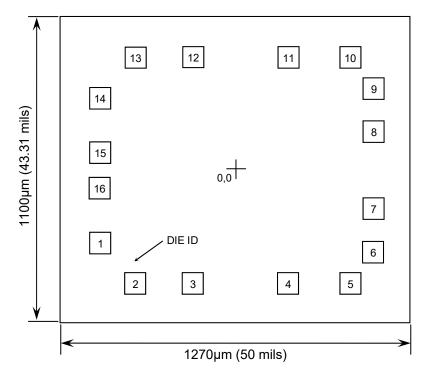
Die Size (Unsawn)	1270 x 1100 50 x 43	μm mils	
Minimum Bond Pad Size	70 x 70 2.76 x 2.76	μm mils	
Die Thickness	280 (±20) 11.02 (±0.79)	μm mils	
Top Metal Composition	Al-Si-Cu		
Back Metal Composition	ack Metal Composition N/A – Bare Si		





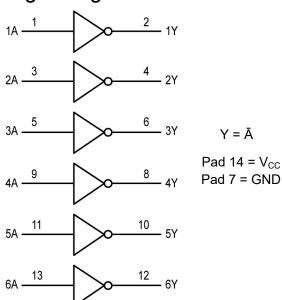
#### Rev 2.0 10/08/25

## Pad Layout and Functions



PAD FUNCTION	FUNCTION	COORDIN	ATES (μm)				
PAD	FUNCTION	X	Υ				
1	1A	-502	-263.5				
2	1Y	-364.9	-410				
3	2A	-157.7	-410				
4	2Y	188.9	-410				
5	3A	413	-410				
6	3Y	495	-298				
7	GND	495	-140				
8	GND	495	140				
9	4Y	495	298				
10	4A	413	410				
11	5Y	188.9	410				
12	5A	-157.7	410				
13	6Y	-364.9	410				
14	6A	-495	263				
15	V <sub>CC</sub>	-495	64.2				
16	V <sub>CC</sub>	-495	-64.2				
CON	CONNECT CHIP BACK TO V <sub>CC</sub> OR FLOAT						

## Logic Diagram



## Truth Table

INPUTS	OUTPUT				
Α	Υ				
Н	L				
L	L H				
H = High level (steady state)					
L = Low level	(steady state)				





# Absolute Maximum Ratings<sup>1</sup>

Rev 2.0 10/08/25

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V <sub>CC</sub>	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V <sub>IN</sub>	-0.5 to V <sub>CC</sub> +0.5	V
DC Output Voltage (Referenced to GND)	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V
DC Input Current	I <sub>IN</sub>	±20	mA
DC Output Current, per pad	I <sub>OUT</sub>	±50	mA
DC Supply Current, V <sub>CC</sub> or GND, per pad	I <sub>CC</sub>	±50	mA
Power Dissipation in Still Air <sup>2</sup>	P <sub>D</sub>	750	mW
Storage Temperature Range	T <sub>STG</sub>	-65 to 150	°C

<sup>1.</sup> Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## Recommended Operating Conditions<sup>3</sup> (Voltages Referenced to GND)

			, ,		,
PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		$V_{CC}$	4.5	5.5	V
DC Input or Output Voltag	е	$V_{IN}$ , $V_{OUT}$	0	V <sub>CC</sub>	V
Operating Temperature Range		T <sub>J</sub>	-40	+85	°C
Output current - High		I <sub>OH</sub>	-	-24	mA
Output current - Low		I <sub>OL</sub>	-	24	mA
Input Rise or Fall rate	V <sub>CC</sub> = 4.5V	Δt/ΔV	0	10	ns/V
(V <sub>IN</sub> from 0.8V to 2V)	V <sub>CC</sub> = 5.5V	ΔυΔν	0	8	115/V

<sup>3.</sup> This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \le (V_{IN} \text{ or } V_{OUT}) \le V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

### DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V <sub>cc</sub>	CONDITIONS	LIMITS			LIMITS	LIMITS	UNITS
	OTHEOL	•66	CONDITIONS	25°C	85°C	FULL RANGE⁴	Oiiiio		
Minimum High-Level	V <sub>IH</sub>	4.5V	$V_{OUT} = 0.1V$	2	2	2	V		
Input Voltage	VIH	5.5V	or V <sub>CC</sub> -0.1V	2	2	2	V		
Maximum Low-Level	V <sub>IL</sub>	4.5V	$V_{OUT} = 0.1V$ or $V_{CC}$ -0.1V	0.8	0.8	0.8	V		
Input Voltage	V IL	5.5V		0.8	0.8	0.8			
Minimum Low-Level Output Voltage		4.5V	Ι <sub>ΟυΤ</sub> = 50μΑ	0.1	0.1	0.1	V		
	V <sub>OL</sub>	5.5V	1001 – 30μΑ	0.1	0.1	0.1	V		
	<b>V</b> OL 4.	4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^5$	0.36	0.44	0.44	V		
		5.5V	$I_{OL} = 24mA$	0.36	0.44	0.44	<b>V</b>		

 <sup>-40°</sup>C ≤ T<sub>J</sub> ≤ +85°C
 All outputs loaded; thresholds on input associated with output under test.





Rev 2.0 10/08/25

### DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V <sub>cc</sub>	CONDITIONS		LIMITS		
	OTHIDOL	STIMBOL VCC CONDITIONS	25°C	85°C	FULL RANGE⁴	UNITS	
		4.5V	Ι <sub>ΟυΤ</sub> = 50μΑ	4.4	4.4	4.4	V
Minimum High-Level	V <sub>OH</sub>	5.5V	1001 – 30μΑ	5.4	5.4	5.4	V
Output Voltage	V OH	4.5V	- 110 - 12 111	3.86	3.76	3.76	V
		5.5V	$I_{OH} = -24mA$	4.86	4.76	4.76	V
Maximum Input Leakage Current	I <sub>IN</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> or GND	±0.1	±1.0	±1.0	μA
Additional Maximum I <sub>CC</sub> / Input	ΔI <sub>CCT</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> -2.1V	0.6	1.5	1.5	mA
Minimum Dynamic	I <sub>OLD</sub>	5.5V	V <sub>OLD</sub> = 1.65V Max	-	75	75	mA
Output Current <sup>6</sup>	I <sub>OHD</sub>	5.5V	V <sub>OHD</sub> = 3.85V Min	-	-75	-75	ША
Maximum Quiescent Supply Leakage Current	I <sub>cc</sub>	5.5V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	4	40	40	μA

<sup>6.</sup> Maximum test duration 2ms, one output loaded at a time.

# AC Electrical Characteristics<sup>7</sup> V<sub>CC</sub> = 5.0V ±0.5V

PARAMETER SYM	SYMBOL	V <sub>cc</sub>	CONDITIONS		LIMIT	S	UNITS
	OTHEOL	• 66	CC	25°C	85°C	FULL RANGE⁴	5.4110
Maximum Propagation Delay	t <sub>PLH</sub>	5.0V	C <sub>L</sub> = 50pF, Input	8.5	9	9	ns
Input A to Output Y (Figure 1)	t <sub>PHL</sub>	5.0V	4. 46 0 0	8	8.5	8.5	113
Maximum Input	C <sub>IN</sub>	5.0V	T <sub>J</sub> = 25°C		TYPIC	AL	pF
Capacitance	2114		1, 200		4.5		Pi
Power Dissipation Capacitance	C <sub>PD</sub>	5.0V	$T_J = 25$ °C, $C_L = 50$ pF		30		pF

<sup>7.</sup> Not production tested in die form, characterized by chip design and tested in package.





Rev 1.1 08/03/21

## Switching Waveform

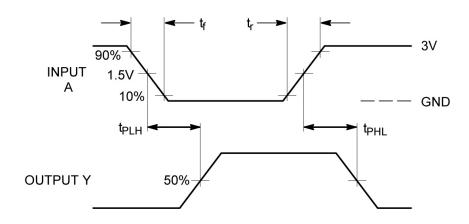
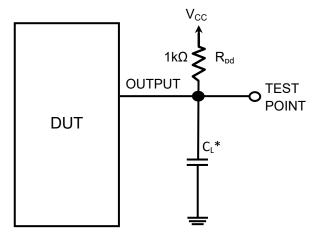


Figure 1 - Propagation delay, Input A to Output Y

#### **Test Circuit**



<sup>\*</sup> Includes all probe and jig capacitance

Figure 2 - Test Circuit

DISCLAIMER: The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Silicon Supplies Ltd hereby disclaims any and all warranties and liabilities of any kind.

LIFE SUPPORT POLICY: Silicon Supplies Ltd components may be used in life support devices or systems only with the express written approval of Silicon Supplies Ltd, if a failure of such components can reasonably be expected to cause the failure of that life support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

